



## PRODUCT SPECIFICATION

# 8124N-P

Wi-Fi 5G band 4x4 11ax

PCIe Module Datasheet

Version:v1.0

**Customer:** \_\_\_\_\_

**Customer P/N:** \_\_\_\_\_

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# 8124N-P Module Datasheet

Ordering Information	Part NO.	Description
	PA8124NPXX-00	QCN9024,5GHz a/n/ac/ax Wi-Fi,4T4R,62.4x57mm,PCIE M.2 E-key,IPEX

Target power:

5.8G: TBD



## CONTENTS

<b>1. General Description</b> .....	<b>5</b>
1.1 Introduction .....	5
1.2 Description .....	5
<b>2. Features</b> .....	<b>6</b>
<b>3. Block Diagram</b> .....	<b>6</b>
<b>4. General Specification</b> .....	<b>7</b>
4.1 5GHz RF Specification .....	7
<b>5. Pin Definition</b> .....	<b>9</b>
5.1 Pin Outline .....	9
5.2 Pin Definition details .....	10
<b>6. Electrical Specifications</b> .....	<b>13</b>
6.1 Power Supply DC Characteristics .....	13
6.2 Power Consumption .....	13
6.3 Interface Circuit time series .....	14
6.3.1 Powerup sequence timing .....	14
<b>7. Size reference</b> .....	<b>14</b>
7.1 Module Picture .....	14
7.2 Marking Description .....	15
7.3 Physical Dimensions .....	15
<b>8. The Key Material List</b> .....	<b>16</b>
<b>9. Reference Design</b> .....	<b>17</b>
<b>10. Recommended Reflow Profile</b> .....	<b>17</b>
<b>11. RoHS compliance</b> .....	<b>17</b>
<b>12. Package</b> .....	<b>18</b>
<b>13. Moisture sensitivity</b> .....	<b>18</b>



# 1. General Description

## 1.1 Introduction

8124N-P is an 802.11ax Wi-Fi 5G PCIe radio, with 802.11ax technology is a highly integrated wireless local area network (WLAN) system-onchip(SoC) for 5 GHz IEEE802.11ax/ac/n/a applications.

The wireless module complies with IEEE 802.11 a/n/ac/ax 4x4 MIMO standard and it can achieve up to a speed of 4804Mbps (4x4 11ax 160Mhz ). The integrated module provides PCIe interface for Wi-Fi,

## 1.2 Description

Model Name	8124N-P
Product Description	Support Wi-Fi functionalities
Dimension	L x W x H: 62.4 x 57 mm
Wi-Fi Interface	Support PCIe E-key
Operating temperature	0°C to 70°C -20°C to 70°C(industrial chip)
Storage temperature	-40°C to 90°C

## 2. Features

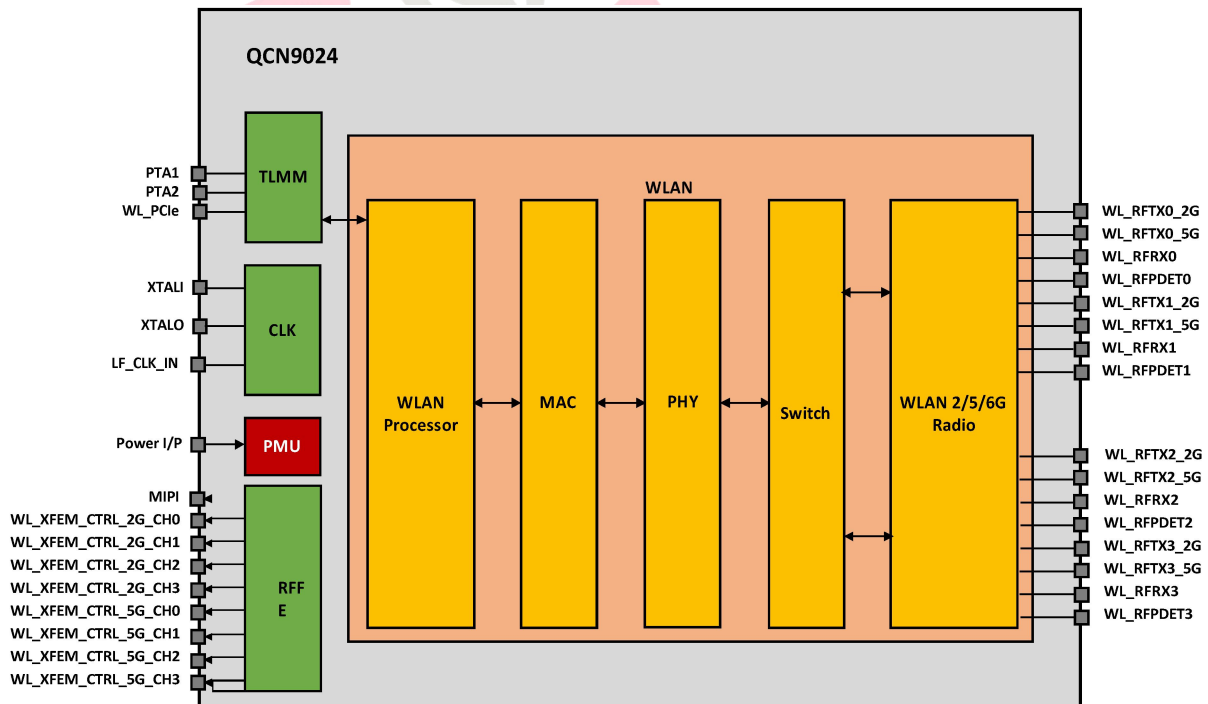
### General

- 4x4/160 MHz 11ax PCIe Radio.
- Supports 20/40/80/160 MHz in 5 GHz.
- Compliant with IEEE 802.11a/n/ac/ax.
- Data rates of up to 4804 Mbps for 160 MHz ax Mode
- Supports up to 256 simultaneously connected clients
- TxBF, MU-MIMO, MU-OFDMA/TxBF, ML, STBC
- IEEE 802.11d, h, i, j, k, r, u, v, and w
- Four interfaces to external PAs operating in the 5 GHz
- WPA/WPA2-Personal/WPA2-Enterprise and WPA3 Personal
- 2Mbit serial I<sup>2</sup>C bus EEPROM

### Host Interface

- Support PCI Express 2-lane-g2 or 1-lane-g3

## 3. Block Diagram



## 4. General Specification

### 4.1 5GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11a/n/ac/ax, Wi-Fi compliant	
Frequency Range	5.15 GHz ~ 5.850 GHz (5 GHz Band)	
Number of Channels	5.0GHz: Please see the table <sup>1</sup>	
Test Items	Typical Value	EVM
Output Power <sup>1</sup>	802.11a /54Mbps: 20 dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7: 20 dBm ± 2 dB	EVM ≤ -28dB
	802.11ac VHT20/MCS8: 16 dBm ± 2 dB	EVM ≤ -30dB
	802.11ac VHT40/MCS9: 16 dBm ± 2 dB	EVM ≤ -32dB
	802.11ac VHT80/MCS9: 16 dBm ± 2 dB	EVM ≤ -32dB
	802.11ax HE20/MCS11: 14 dBm ± 2 dB	EVM ≤ -35dB
	802.11ax HE40/MCS11: 14 dBm ± 2 dB	EVM ≤ -35dB
	802.11ax HE80/MCS11: 13 dBm ± 2 dB	EVM ≤ -35dB
802.11ax HE160/MCS11: 13 dBm ± 2 dB	EVM ≤ -35dB	
Test Items	Test Value	Standard Value
SISO Receive Sensitivity (11a,20MHz) @10% PER	- 6Mbps @ -90 dBm	≤ -82 dBm
	- 54Mbps @ -71 dBm	≤ -68 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤ -82 dBm
	- MCS=7 @ -69 dBm	≤ -67 dBm
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤ -79 dBm
	- MCS=7 @ -66 dBm	≤ -64 dBm
SISO Receive Sensitivity (11ac,20MHz)@10% PER	- MCS=0, NSS1 @ 90 dBm	≤ -82 dBm
	- MCS=8, NSS1 @ -64 dBm	≤ -60 dBm
SISO Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0, NSS1 @ -87 dBm	≤ -79 dBm
	- MCS=9, NSS1 @ -59 dBm	≤ -55 dBm
SISO Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0, NSS1 @ -84 dBm	≤ -76 dBm
	- MCS=9, NSS1 @ -56 dBm	≤ -54 dBm
SISO Receive Sensitivity (11ax,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤ -82 dBm
	- MCS=11 @ -60 dBm	≤ -52 dBm
SISO Receive Sensitivity (11ax,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤ -79 dBm
	- MCS=11 @ -57 dBm	≤ -49 dBm
SISO Receive Sensitivity (11ax,80MHz) @10% PER	- MCS=0 @ -84 dBm	≤ -76 dBm
	- MCS=11 @ -54 dBm	≤ -46 dBm

SISO Receive Sensitivity (11ax,160MHz) @10% PER	- MCS=0 @ -81 dBm	≤-73 dBm
	- MCS=11 @ -51 dBm	≤-43 dBm
Maximum Input Level	802.11a/n: -30 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

1. output power may update in future version,and is defined by driver bin file, please check with FNLINK.

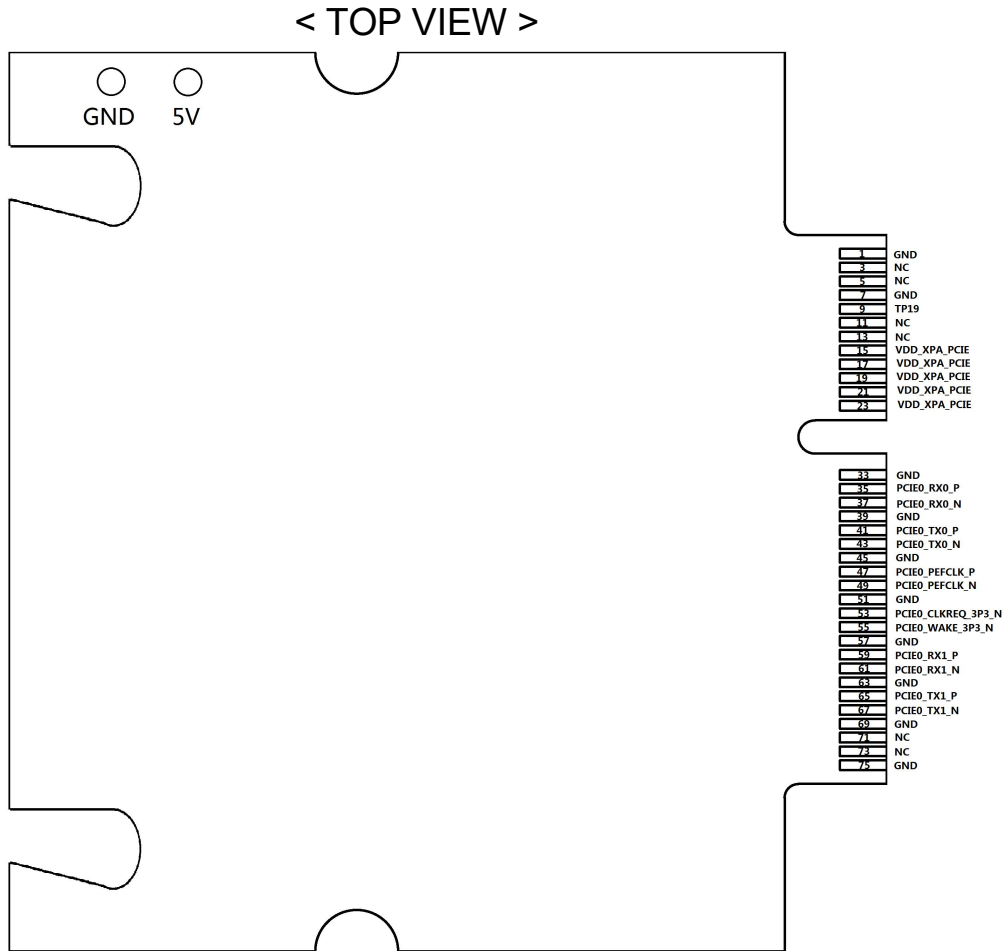
**15GHz(20MHz) Channel table**

Band range	Operating Channel Numbers	Channel center frequencies(MHz)
5150MHz~5250MHz	36	5180
	40	5200
	44	5220
	48	5240
5250MHz~5350MHz	52	5260
	56	5280
	60	5300
	64	5320
5470MHz~5725MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
140	5700	
5725MHz~5850MHz	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

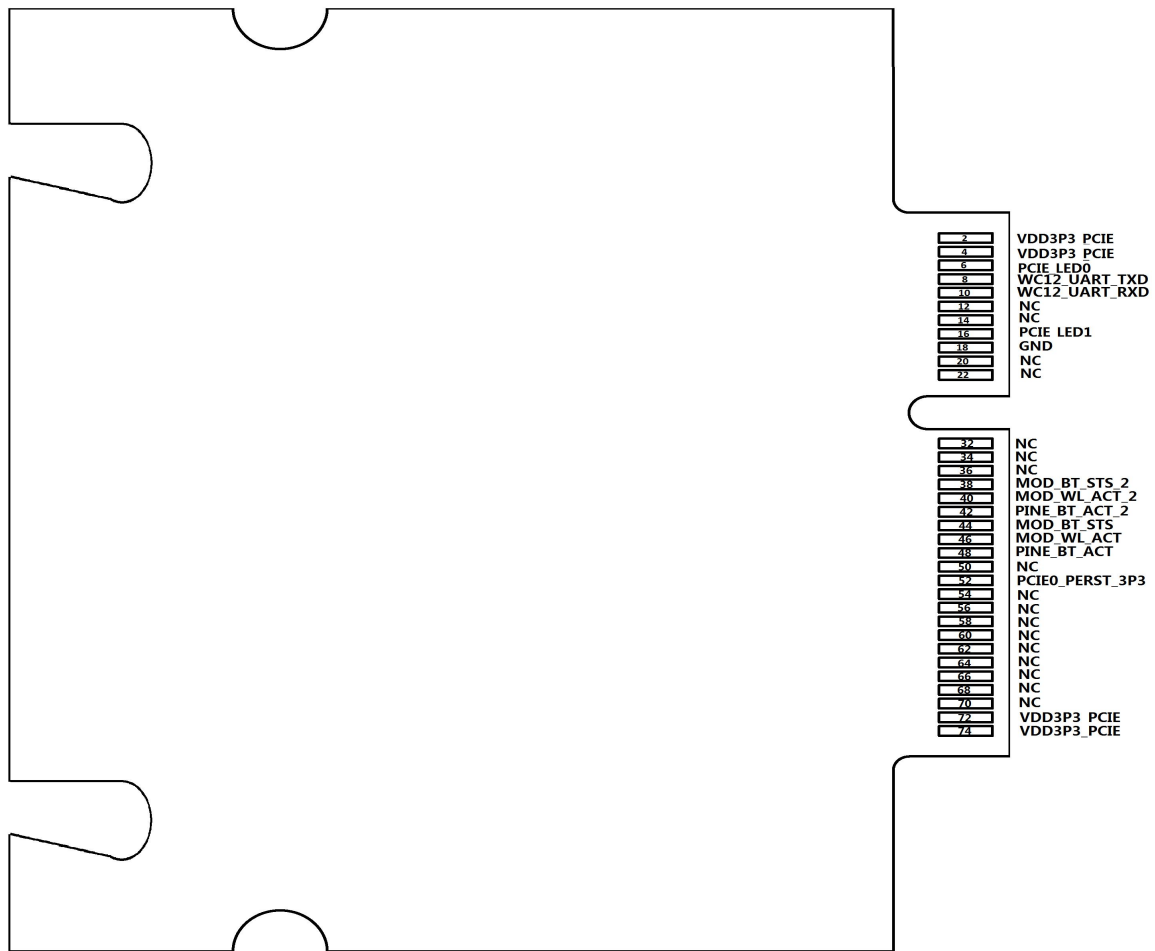


## 5. Pin Definition

### 5.1 Pin Outline



< BOTTOM VIEW >



### 5.2 Pin Definition details

TOP

NO.	Name	Type	Description	Voltage
1	GND	—	Ground connections	
3	NC	—	No connect	
5	NC	—	No connect	
7	GND	—	Ground connections	
9	TP19	—	No connect	
11	NC	—	No connect	
13	NC	—	No connect	

15	VDD_XPA_PCIE	P	Power supply for PA	5V
17	VDD_XPA_PCIE	P	Power supply for PA	5V
19	VDD_XPA_PCIE	P	Power supply for PA	5V
21	VDD_XPA_PCIE	P	Power supply for PA	5V
23	VDD_XPA_PCIE	P	Power supply for PA	5V
33	GND	—	Ground connections	
35	PCIE0_RX0_P	I	WLAN PCIe L0 receive input differential signals	1.8V
37	PCIE0_RX0_N	I	WLAN PCIe L0 receive input differential signals	1.8V
39	GND	—	Ground connections	
41	PCIE0_TX0_P	O	PCIe L0 transmit output differential signals	1.8V
43	PCIE0_TX0_N	O	PCIe L0 transmit output differential signals	1.8V
45	GND	—	Ground connections	
47	PCIE0_REFCLK_P	I	PCIe reference clock input differential signals	1.8V
49	PCIE0_REFCLK_N	I	PCIe reference clock input differential signals	1.8V
51	GND	—	Ground connections	
53	PCIE0_CLKREQ_3P3_N	B	PCIe clock request signal is a bidirectional signal. It is an open-drain signal that requires an external 10 K $\Omega$ pull-up resistor.	1.8V
55	PCIE0_WAKE_3P3_N	O/B	PCIe wake-up signal is an output signal. It is an open-drain signal that requires an external 10 K $\Omega$ pull-up resistor.	1.8V
57	GND	—	Ground connections	
59	PCIE0_RX1_P	I	PCIe L1 receive input differential signals	1.8V
61	PCIE0_RX1_N	I	PCIe L1 receive input differential signals	1.8V
63	GND	—	Ground connections	
65	PCIE0_TX1_P	O	PCIe L1 transmit output differential signals	1.8V
67	PCIE0_TX1_N	O	PCIe L1 transmit output differential signals	1.8V
69	GND	—	Ground connections	
71	NC	—	No connect	
73	NC	—	No connect	
75	GND	—	Ground connections	

**BOTTOM**

<b>NO.</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>	<b>Voltage</b>
2	VDD3P3_PCIE	P	3.3V main power supply	3.3V
4	VDD3P3_PCIE	P	3.3V main power supply	3.3V

6	PCIE_LED0	O	LED interface 0 for RFA debug. GPIO27	1.8V
8	WC12_UART_TXD	-	NC, no function pin connected.	
10	WC12_UART_RXD	-	NC, no function pin connected.	
12	NC	—	No connect	
14	NC	—	No connect	
16	PCIE_LED1	O	LED interface 1.GPIO35	1.8V
18	GND	—	Ground connections	
20	NC	—	No connect	
22	NC	—	No connect	
32	NC	—	No connect	
34	NC	—	No connect	
36	NC	—	No connect	
38	MOD_BT_STS_2	-	No connect	
40	MOD_WL_ACT_2	-	No connect	
42	PINE_BT_ACT_2	-	No connect	
44	MOD_BT_STS	I	Wi-Fi coexistence with Bluetooth priority signal PTA 1.GPIO41	1.8V
46	MOD_WL_ACT	O	WLAN active signal PTA 1.GPIO42	1.8V
48	PINE_BT_ACT	I	Wi-Fi coexistence with Bluetooth active signal PTA 1.GPIO40	1.8V
50	NC	—	No connect	
52	PCIE0_PERST_3P3	I	PCIe reset signal is an input signal.	1.8V
54	NC	—	No connect	
56	NC	—	No connect	
58	NC	—	No connect	
60	NC	—	No connect	
62	NC	—	No connect	
64	NC	—	No connect	
66	NC	—	No connect	
68	NC	—	No connect	
70	NC	—	No connect	
72	VDD3P3_PCIE	P	3.3V main power supply	3.3V
74	VDD3P3_PCIE	P	3.3V main power supply	3.3V

P:POWER I:INPUT O:OUTPUT

## 6. Electrical Specifications

### 6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VDD_XPA_PCIE	4.5	5.0	5.5	V
VDD3P3_PCIE	3.0	3.3	3.6	V

### 6.2 Power Consumption

Power Consumption	VCC(Unit:mA)	
5G TX (HE80 11ax)		TBD
5G RX (HE80 11ax)		
5G TX (VHT80 11ac)		
5G RX (VHT80 11ac)		
2.4G TX (HE40 11ax)		
2.4G RX(HE40 11ax)		
2.4G TX (HT40 11n)		
2.4G RX (HT40 11n)		
2.4G TX (OFDM 54M)		
2.4G RX (OFDM 54M)		

### 6.3 Interface Circuit time series

#### 6.3.1 Powerup sequence timing

This section describes the PMIC that includes power-on circuits that provide the proper power sequencing for the entire QCN9024 chipset. Alternatively, instead of PMIC regulators, discrete SMPS design can also be used with power sequence requirement of this chipset.

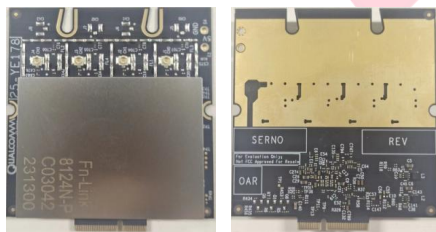


NOTE: The power supply reaches 90% of final voltage before the next supply is enabled.

## 7. Size reference

### 7.1 Module Picture

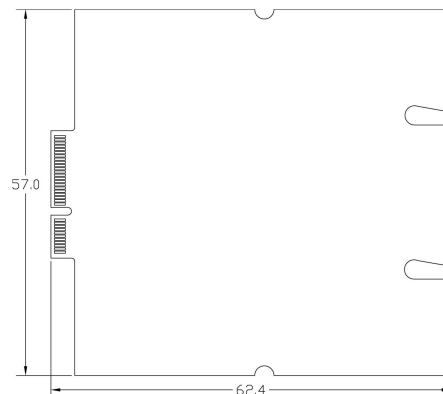
L x W : 62.4 x 57 (+0.3/-0.1) mm



镭雕丝印后续将更新方向如 7.2 图

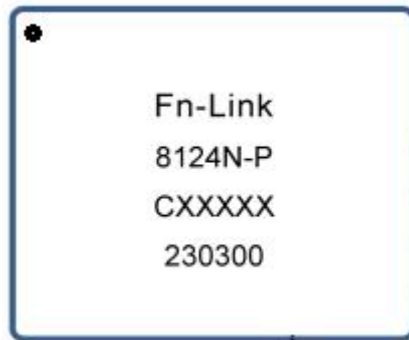
H: 7.5 (±0.2) mm

**Weight**



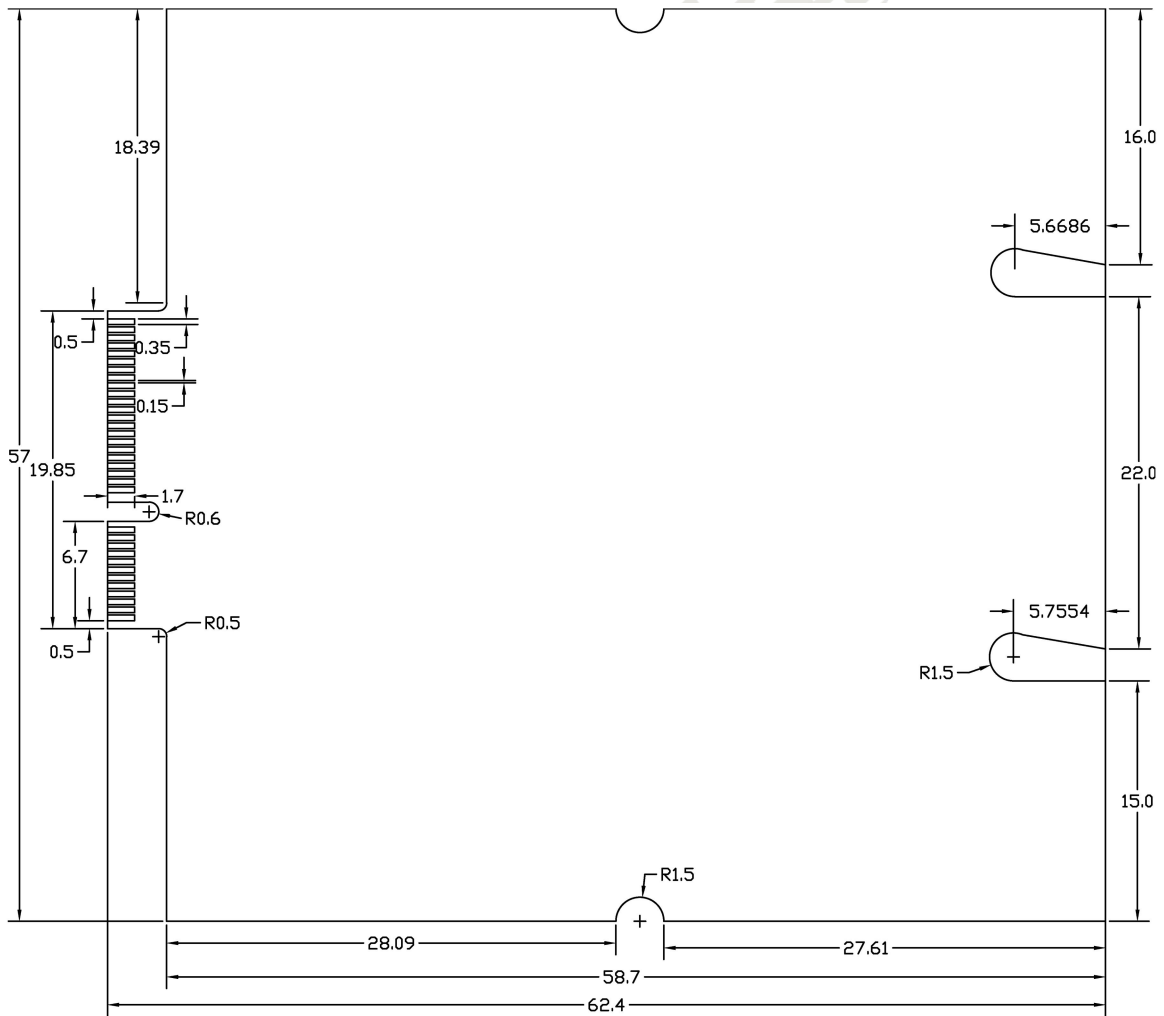
15.2g

### 7.2 Marking Description

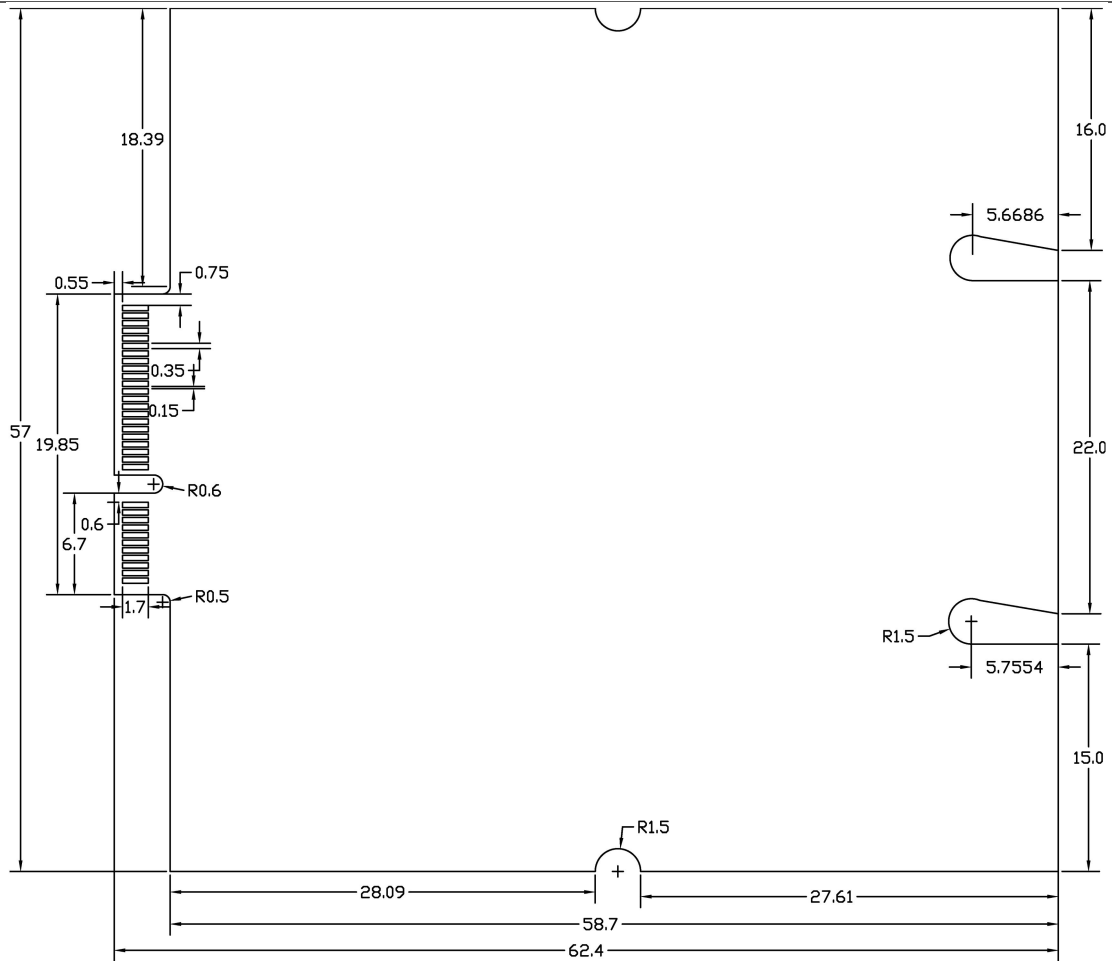


### 7.3 Physical Dimensions

<TOP View>



<BOTTOM View>



## 8. The Key Material List

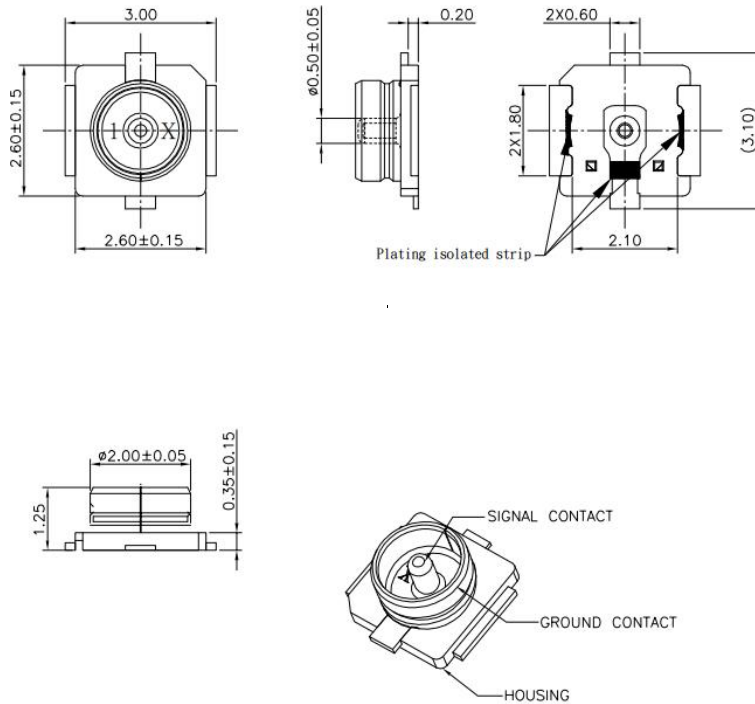
Item	Part Name	Description	Manufacturer
1	Inductor	2016 1.0uH,±20%,DCR 0.046Ω,Irms=3.4A/Isat=4.6A	Sunlord,Ceaiya,cenker,TAIYO,Chilisin,INPAQ
2	IPEX	1代 RF CONN GEN I W NOTCH	启明盛,佳沃,电连,创迪尔
3	Crystal	2016 48MHz 9.9pF ±20ppm	ECEC, TKD, Hosonic, JWT, TXC
4	Chipset	QCN-9024-0-MSP234-TR-01-0	Qualcomm
5	PCB	8124N-P,IPC 三级,4L,FR4,,62.4X57X0.8mm,	XY-PCB,GDKX,Sunlord,SL-PCB,TRULY
6	Shielding	8124N-P,shielding	信太,精力通,卓益
7	FEM	5GFEM,WIFI6,5V	Qorvo,KX,skyworks
8	Power IC	DC-DC /LDO	MPS,芯创, FITIPOWER,



## 9. Reference Design

A. Antenna connector as below spec.

B. For better heat dissipation, it is recommended to add heat sink on top of the shielding and thermal pad on bottom side.



## 10. Recommended Reflow Profile

no reflow process.

## 11. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

## 12. Package

TBD

## 13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH)
- b) Environmental condition during the production:  $30^{\circ}\text{C}$  / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
- e) Baking is required if conditions b) or c) are not respected
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more