



Product Specification

3121N-IEE

PLC-IoT Module

Version: v3.1 (PE0211)

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL: +86-755-2955-8186

Website: www.fn-link.com

3121N-IEE Module Datasheet

Ordering Information	Part NO.	Description
	FG3121NIEE-01	PE0211, 92.8*63.8mm, three-phase CCO, Extended IO
	FG3121NIEE-02	PE0211, 92.8*63.8mm, three-phase CCO, QGDW 1375.2-2019 Standard IO

CONTENTS

1. General Description.....	5
1.1 Introduction.....	5
1.2 Features.....	5
1.3 General Specification.....	6
1.4 Recommended Operation Condition.....	6
2. Module PIN Definition.....	7
2.1 Module Picture.....	7
2.2 PIN Distribution.....	7
2.3 PIN Definition.....	8
2.4 Connector Specifications.....	9
3. Hardware Design Guide.....	10
3.1 Voltage Input.....	10
3.2 PLC Peripheral Design.....	10
3.3 Typical PLC network.....	12
4. Key Material List.....	12
5. RoHS compliance.....	12
6. Package.....	13
7. Moisture sensitivity.....	13

Revision History

Version	Date	Contents	Draft	Checked	Approved
V1.0	2020/12/09	Initial release	FC	LSP	QJP
V2.0	2021/01/27	Update the module and connector drawing and add photos	FC	LSP	QJP
V2.1	2021/05/27	Correct known typos.	FC	LSP	QJP
V3.0	2022/08/19	PE0211 chip version	FC	TZ	QJP
V3.1	2023/01/14	Apply the format of the new specification; Update ordering information; Correct known typos.	FC	LSP	QJP

1. General Description

1.1 Introduction

3121N-IEE is a highly integrated Power Line Communication (PLC) module for IoT and electrical power system applications. It is integrated with multi-mode power line communication modem, a built-in line driver and an ARM Cortex-M3 MCU. The module is compliant with IEEE P1901.1 standard and supports OFDM/FSK modulation.

3121N-IEE provides a DC interface and an AC interface with DIP headers. The DC interface is consist of DC power supply, UART, ADC and GPIOs; while AC interface is for PLC communication. This module is a good solution for intelligent street lighting, energy management, intelligent meter reading applications.

The module size and interface are compliant with QGDW 1375.2-2019 standard.

1.2 Features

CPU and storage

- High efficient Cortex-M3 processor, operating at up to 200MHz frequency
- Built-in SRAM 256KB
- 2MB Flash

PHY Characteristics

- Support IEEE 1901.1
- Support frequency band 0.5-3.7MHz and 2.5-5.7MHz, software configurable
- Support OFDM (Orthogonal Frequency Division Multiplex) technology, BPSK (Binary Phase Shift Keying) and QPSK (Quadrature Phase Shift Keying) modulation
- Support FEC (Forward Error Correction) and CRC (Cyclic Redundancy Check)

MAC Characteristics

- Support TDMA (Time Division Multiple Access) and CSMA(Carrier Sense Multiple Access)/CA (Collision Avoidance), provides conflict-avoid ability
- Support data segmentation and reorganization, increase data transmission efficiency
- Support data retransmission
- Support QoS (Quality of Service)

PLC Network Characteristics

- Support fast self-organization network. A typical 2 level network with 200 devices can be ready to communicate in less than 10 seconds
- Support Dynamic Routing and Multipath addressing

Peripheral Interfaces

- UART, GPIO, ADC

Network Performance

- Physical layer rate up to 0.507Mbps, application layer rate up to 80Kbps
- Receiving Sensitivity better than 0.2mVpp, about 95dB anti-attenuation performance

Power Consumption and Others

- Idle consumption $\leq 1W$ (networked but no communication)
- Dynamic working consumption $\leq 1.5W$
- Operation temperature: $-40^{\circ}C \sim +85^{\circ}C$
- Storage temperature: $-40^{\circ}C$ to $125^{\circ}C$

1.3 General Specification

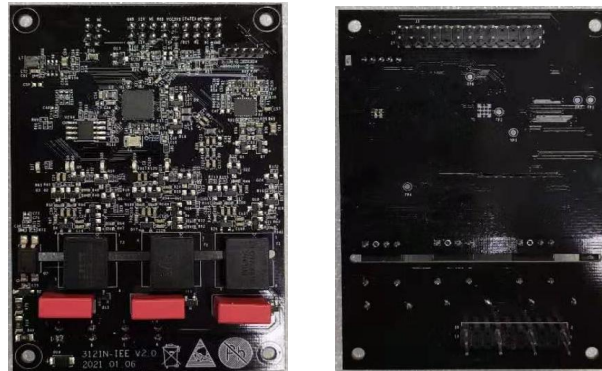
Model Name	3121N-IEE
Main Chip	PE0211
Interfaces	PLC, UART, GPIO, ADC
Communication mode	Power Line Communication
Dimension	L x W : 92.8*63.8mm

1.4 Recommended Operation Condition

Input Voltage	12Vdc $\pm 3\%$
Operation Temperature	$-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature	$-40^{\circ}C$ to $+125^{\circ}C$

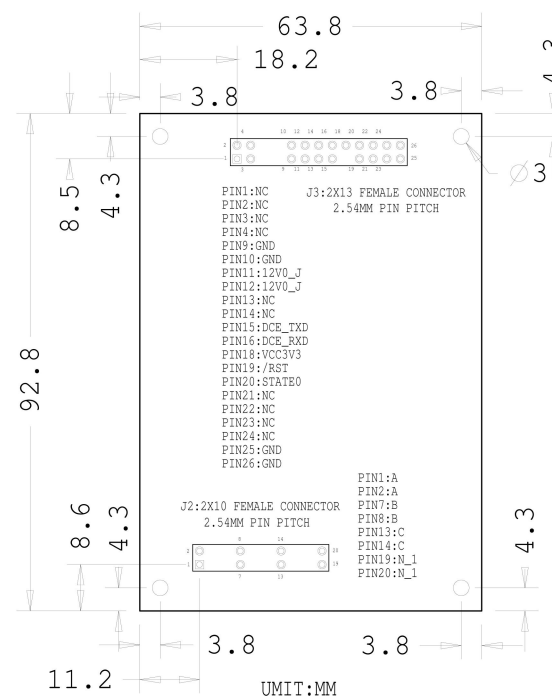
2. Module PIN Definition

2.1 Module Picture



2.2 PIN Distribution

<Top View>



Note: Headers are mounted on the bottom side of the module.

2.3 PIN Definition

J1 Interface (13x2 pin , 2.54mm pitch), DC interface		
NO.	Name	Description
1	GPIO11	FG3121NIEE-01: GPIO_11, can be configured as UART RTS. FG3121NIEE-02: NC
2	GPIO12	FG3121NIEE-01: GPIO_12, can be configured as UART CTS. FG3121NIEE-02: NC
3	GPIO3	FG3121NIEE-01: GPIO_3 FG3121NIEE-02: NC
4	GPIO19	FG3121NIEE-01: GPIO_19 FG3121NIEE-02: NC
5-8	NC	Floating pins, no header
9-10	GND	Ground connections
11-12	12V0_J	DC 12V power input
13-14	NC	Floating
15	DCE_TXD	UART0 output, 3.3V power domain, can be configured as GPIO_8.
16	DCE_RXD	UART0 input, 3.3V power domain, can be configured as GPIO_7.
17	NC	Floating pins, no header
18	VCC3V3	Floating
19	/RST	Reset input, active low. 3.3V power domain.
20	STATE0	Module insertion indicator, low level indicates module inserted
21	NC	Floating
22	VIN5	FG3121NIEE-01: ADC input, measurable voltage range 0.1~2.75V, resolution 12bit FG3121NIEE-02: NC
23	GPIO1	FG3121NIEE-01: GPIO_1. FG3121NIEE-02: NC
24	GPIO2	FG3121NIEE-01: GPIO_2. FG3121NIEE-02: NC
25-26	GND	Ground connections

Remark 1: IO power domain 3.3V.

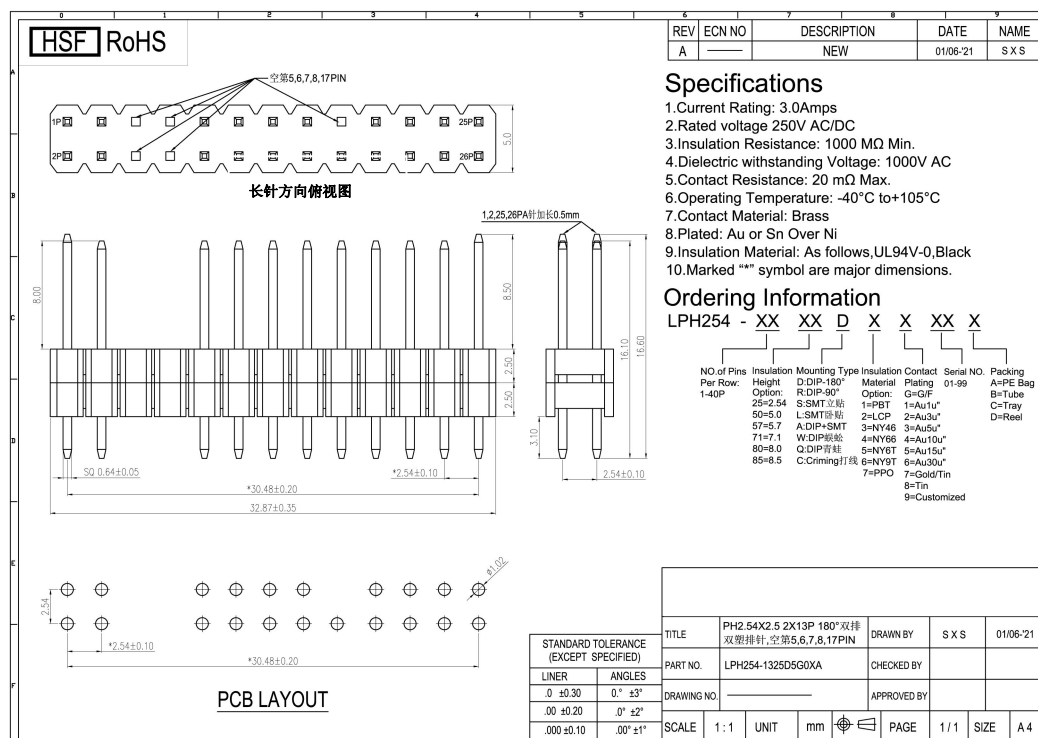
Remark 2: FG3121NIEE-02 is fully compatible with the local communication module pin requirements that defined in QGDW 1375.2-2019 standard. While FG3121NIEE-01 is an extended IO version for some

customization requirements.

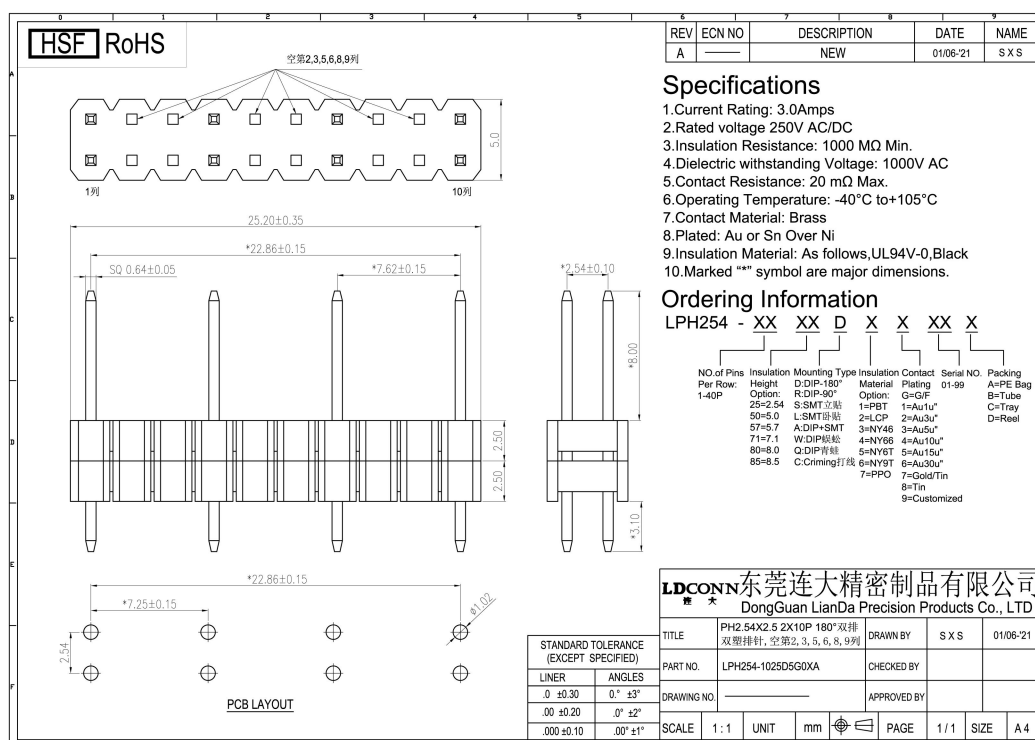
J2 Interface (10x2 pin, 2.54mm pitch), AC interface		
NO.	Name	Description
1-2	A	A wire of three-phase electrical power line
3-6	NC	No connection, no header, for safety isolation
7-8	B	B wire of three-phase electrical power line
9-12	NC	No connection, no header, for safety isolation
13-14	C	C wire of three-phase electrical power line
15-18	NC	No connection, no header, for safety isolation
19-20	N	Neutral wire of three-phase electrical power line

2.4 Connector Specifications

Header of DC interface:13x2pin, pitch 2.54mm



Header of AC interface: 10x2pin, pitch 2.54mm



3. Hardware Design Guide

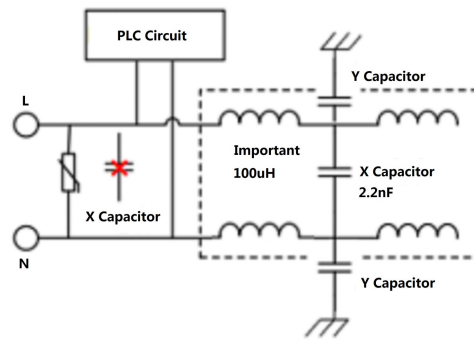
3.1 Voltage Input

ITEM	Min.	Typ.	Max.	Unit
DC 12V input voltage	11.64	12	12.36	V

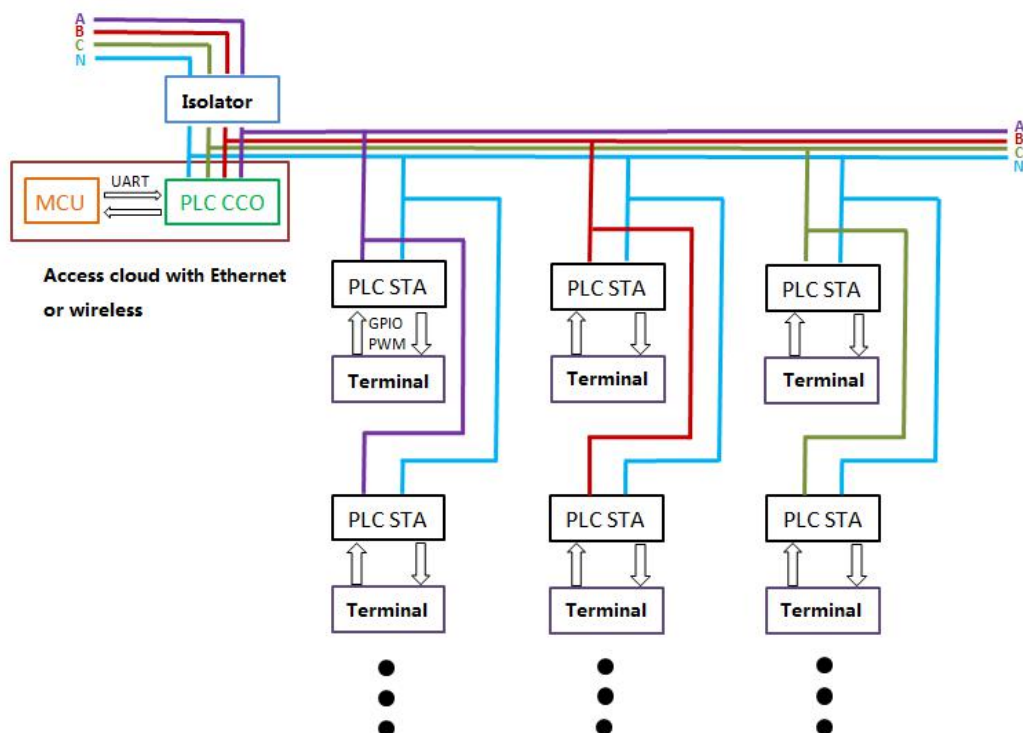
- Put a 22uF and a 0.1uF capacitor close to module's 12V input pin. Keep power ripple less than 720mVpp.
- Make sure the current supply is greater than 120mA for 12V input.

3.2 PLC Peripheral Design

The circuit design of AC input, especially AC/DC part may strongly impact the performance of PLC. Some design guidelines are listed as below.



- After AC/DC power converter is applied, if the distance between CCO and 1st level STA (PCO) is less than 50m, make sure the noise floor of 500kHz~6MHz is less than -110dBm/Hz; if the distance is more than 50m, the noise should be less than -120dBm/Hz.
- To minimize path attenuation of PLC signal, component with more than 600pF capacitance is not allowed at the "x" marked position of above picture. (Consider total capacitance if several components in parallel).
- If the end product must implement X capacitor to suppress the differential noise on L-N power line, it is recommended to serial in 100uH inductors on both L&N then place the X capacitor behind the inductors. This design can also increase the impedance of the PLC frequency band and reduce the attenuation of PLC signal. The recommended capacitance of X capacitor is 2.2nF (lower the capacitance will bring better PLC performance). If Y capacitor is needed, please also place it/them behind the inductor (minimize the capacitance of Y capacitor as well, but usually the impact of Y capacitor is less than X capacitor).
- Please never use common-mode choke instead of above 100uH differential inductor. PLC is a kind of differential signal, so common-mode choke is not able to isolate the attenuation of X capacitor.
- If DCDC convertor is applied, the recommended switch frequency is less than 1MHz. Suppress out-of-band noise to reduce EMI risk and get better PLC performance.
- Chose proper MOV and Fuse according to the specification of end product, MOV's parasitic capacitance should be as lower as possible.
- Make sure MOV is in front of both PLC circuit and AC-DC convertor to get best protection.
- While installing the module, pay attention to safety requirements.
- PLC circuit's RX channel, especially filter and coupler, might couple electromagnetic interference then worsen PLC performance. So please keep all interference source (DC-DC for example) far away from RX circuit.



Item	Part Name	Description	Manufacturer
1	Chipset	PE0211, QFN-56, 7*7mm	
2	Crystal	3225, 25MHz, 10ppm	ECEC, TKD, Hosonic, JWT, TXC
3	Flash	SPI NOR, 2MB, SOP8	MXIC, Winbond, GigaDevice, XTX
4	PCB	FR4, 2 Layers, Black	XY-PCB, Sunlord, GDKX, SL-PCB
5	Line Driver	HPLC Line driver, 8~32V, QFN24	TI, WILLSEMI

All hardware components are fully compliant with EU RoHS directive.

6. Package

TBD.

7. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
- e) Baking is required if conditions b) or c) are not respected
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more